In the Claims:

Please cancel claim 17.

Please amend the below claims as indicated.

1. (Original) A method for transferring data comprising:

providing a master request bus;

providing a slave request bus;

initiating an operation utilizing a protocol when a master request and an arbiter grant is received from the master request bus;

wherein the protocol enables transfer of data between computer hardware operating according to different protocols.

2. (Currently Amended) A method for transferring data, ~~The method for transferring data according to claim 1, further~~ comprising:

providing a master request bus;

providing a slave request bus;

initiating an operation utilizing a protocol when a master request and an arbiter grant is received from the master request bus;

wherein the protocol enables transfer of data between computer hardware operating according to different protocols;

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to an analysis machine;

classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator.

3. (Currently Amended) The method for transferring data according to claim 2 ~~1~~, further comprising transferring the data after modifying and forwarding to an output buffer.

4. (Currently Amended) The method for transferring data according to claim 2 ~~1~~, further comprising processing data packets at a rate of at least 10 Gbs.

5. (Original) A global access bus for transferring data, said global access bus comprising:

a master request bus; and

a slave request bus operationally connected to said master request bus;

wherein said master request bus and said slave request bus utilize a protocol enabling transfer of data between computer hardware operating according to different protocols.

6. (Currently Amended) A global access bus for transferring data, ~~according~~ and associated apparatus, ~~to claim 5, in combination with an apparatus~~ comprising:

a master request bus;

a slave request bus operationally connected to said master request bus;

wherein said master request bus and said slave request bus utilize a protocol enabling transfer of data between computer hardware operating according to different protocols;

an analysis machine having multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field;

a packet task manager operationally connected to said analysis machine; and,

a packet manipulator operationally connected to said analysis machine.

7. (Original) The apparatus according to claim 6, wherein said analysis machine is multi-threaded.

8. (Original) The apparatus according to claim 6, wherein said analysis machine has 32 threads.

9. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

a packet task manager operationally connected to said analysis machine; and

a packet manipulator operationally connected to said analysis machine.

10. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

an external memory engine operationally connected to said analysis machine; and

a hash engine operationally connected to said analysis machine.

11. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

packet input global access bus software code used for flow of data packet information from a flexible input data buffer to an analysis machine.

12. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

packet data global access bus software code used for flow of packet data between a flexible data input bus and a packet manipulator.

13. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

statistics data global access bus software code used for connection of an analysis machine to a packet manipulator.

14. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

private data global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

15. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

lookup global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

16. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

results global access bus software code used for providing flexible access to an external memory.

17. (Cancelled)

18. (Currently Amended) The apparatus according to claim 6 ~~5~~, further comprising:

a bi-directional access port operationally connected to said analysis machine;

a flexible data input buffer operationally connected to said analysis machine; and

a flexible data output buffer operationally connected to said analysis machine.